IN THE CLAIMS:

Please amend the claims as follows:

1-5. (Cancelled)

6. (Currently amended) A data processing method comprising the steps of:

writing a processing specification information in a first area corresponding to a first word line within a semiconductor device comprising at least one memory array and a ~~data processor~~ reconfigurable logic circuit coupled to said at least one memory array through at least one internal data bus;

writing data to be processed in a second area corresponding to a second word line, which is different from the first word line, within said semiconductor device;

transferring said processing specification information through said at least one internal data bus in parallel ~~in a batch~~ to said reconfigurable logic circuit, said processing specification information determining logical connections of said reconfigurable logic circuit ~~data processor~~;

transferring said data through said at least one internal data bus in parallel ~~in a batch~~ to said reconfigurable logic circuit ~~data processor~~;

processing said data by said reconfigurable logic circuit according to ~~data processor using~~ said processing specification information and writing resultant processed data through said at least one internal data bus in parallel ~~in a batch~~ in a third area corresponding to a third word line within said semiconductor device; and

obtaining said resultant processed data by reading said third area after writing said resultant processed data.

7. (Cancelled)

8. (Previously presented) The data processing method of claim 6,

wherein said second area and said third area are the same area, and

said semiconductor device overwrites said resultant processed data in said second area where said data has been written.

9. (Previously presented) The data processing method of claim 6, wherein a controller reads time information required for said processing to be executed, and reads said resultant processed data written in said third area on the basis of said read time information after a time corresponding to said time information elapses.

10. (Original) The data processing method of claim 9, wherein said semiconductor device is connected with said controller through a memory network, and said controller stores time information required for each processing to be executed by said semiconductor device.

11. (Previously presented) The data processing method of claim 6, wherein, immediately before executing said processing by said semiconductor device having the data processing function, information describing said processing to be executed is dynamically rewritten for executing said processing.

12-20. (Cancelled)

21. (Previously presented) The data processing method of claim 10, wherein said memory network has a ring network structure.

22. (Previously presented) The data processing method of claim 10, wherein said memory network has a bus network structure.

23-24. (Cancelled)